

**AMENDMENTS TO THE CLAIMS:**

This listing of claims will replace all prior versions, and listings, of claims in the application:

**Listing of Claims:**

1. **(currently amended)** An electrostatic discharge (ESD) protection device, applied to a mixed voltage circuit assembly with independent first and second power supplies, wherein the ~~[[a]]~~ first power supply ~~[[that]]~~ has a high voltage source and a low voltage source and ~~[[a]]~~ the second power supply ~~[[that]]~~ has a high voltage source and a low voltage source, said device comprising:

a RC controlled circuit subassembly, coupled with said mixed voltage circuit assembly, utilizing for substantially controlling said ESD protection device to be ON or OFF, wherein said RC controlled circuit subassembly comprising:

a resistance, one end of said resistance coupled to the high voltage source of said first power supply; and

a capacitor, one end of said capacitor coupled to the low voltage source of said second power supply and the other end of said capacitor coupled to said resistance; and

a first transistor, the source electrode of said first transistor coupled to the high voltage source of said first power supply, the drain electrode of said first transistor coupled to the high voltage source of said second power supply and the gate electrode coupled to said RC controlled circuit subassembly for providing a current route between the high voltage source of said first power supply and the high voltage source of said second power supply on an ESD event, wherein said RC controlled circuit is used to control said first transistor to be ON or OFF.

2. (canceled)

3. **(currently amended)** The device as recited in claim ~~[[2]]~~ 1, wherein the RC time constant of said resistance and said capacitor is about 0.1 to 10  $\mu$ sec.

4. **(currently amended)** The device as recited in claim [[2]] 1, wherein said first transistor is a first PMOS transistor, the gate of said first PMOS transistor being coupled between said resistance and said capacitor, the source of said first PMOS transistor being coupled to the high voltage source of said first power supply, the drain of said first PMOS transistor being coupled to the high voltage source of said second power supply.

5. (original) The device as recited in claim 4, wherein said first PMOS transistor is further located in a first N-well, said first N-well being coupled to the high voltage source of said first power supply.

6. **(currently amended)** An electrostatic discharge (ESD) protection device, applied to a mixed voltage circuit assembly with a first power supply that has a high voltage source and a low voltage source and a second power supply that has a high voltage source and a low voltage source, said device comprising:

a RC controlled circuit subassembly, coupled with said mixed voltage circuit assembly, utilizing for substantially controlling said ESD protection device to be ON or OFF, wherein said RC controlled circuit subassembly comprising:

a resistance, one end of said resistance coupled to the high voltage source of said first power supply; and

a capacitor, one end of said capacitor coupled to the low voltage source of said second power supply and the other end of said capacitor coupled to said resistance; and

a first transistor, the source electrode of said first transistor coupled to the high voltage source of said first power supply, the drain electrode of said first transistor coupled to the high voltage source of said second power supply and the gate electrode coupled to said RC controlled circuit subassembly for providing a current route between the high voltage source of said first power supply and the high voltage source of said second power supply on an ESD event, wherein said RC controlled circuit is used to control said first transistor to be ON or OFF;

wherein

said first transistor is a first PMOS transistor, the gate of said first PMOS transistor being coupled between said resistance and said capacitor, the source of said first PMOS transistor

being coupled to the high voltage source of said first power supply, the drain of said first PMOS transistor being coupled to the high voltage source of said second power supply;

said first PMOS transistor is further located in a first N-well, said first N-well being coupled to the high voltage source of said first power supply; and

said device further comprises ~~The device as recited in claim 5, further comprising~~ a second PMOS transistor located in a second N-well, the gate of said second PMOS transistor being coupled to the low voltage source of said second power supply, the source of said second PMOS transistor and said second N-well being coupled to the drain of said first PMOS transistor, the drain of said second PMOS transistor being coupled to the high voltage source of said second power supply.

7. (previously presented) An electrostatic discharge (ESD) protection device, applied to a mixed voltage circuit assembly with a first power supply that has a high voltage source and a low voltage source and a second power supply that has a high voltage source and a low voltage source, said device comprising: a RC controlled circuit subassembly, coupled with said mixed voltage circuit assembly, utilizing for substantially controlling said ESD protection device to be ON or OFF, wherein said RC controlled circuit subassembly comprising:

a first capacitor, one end of said first capacitor being coupled to the high voltage source of said first power supply; and

a first resistance, one end of said first resistance coupled to the low voltage source of said second power supply and the other end of said first resistance coupled to the first capacitor;

a first transistor, the source electrode of said first transistor coupled to the high voltage source of said first power supply, the drain electrode of said first transistor coupled to the high voltage source of said second power supply and the gate electrode coupled to said RC controlled circuit subassembly for providing a current route between the high voltage source of said first power supply and the high voltage source of said second power supply on an ESD event, wherein said RC controlled circuit is used to control said first transistor to be ON or OFF.

8. (original) The device as recited in claim 7, wherein the RC time constant of said first resistance and said first capacitor is about 0.1 to 10  $\mu$ sec.

9. (original) The device as recited in claim 8, wherein said first transistor is a first NMOS transistor, the gate of said first NMOS transistor being coupled between said first capacitor and said first resistance, the drain of said first NMOS transistor being coupled to the high voltage source of said first power supply, the source of said first NMOS transistor being coupled to the high voltage source of said second power supply.

10. (previously presented) The device as recited in claim 9, wherein said first NMOS transistor is further located in a P-well, said P-well, located in a N-well, being coupled to the high voltage source of said first power supply.

11. (original) The device as recited in claim 9, further comprising a second NMOS transistor, coupled between said first power supply and said second power supply of said mixed voltage circuit assembly, wherein said second NMOS transistor is coupled to said RC controlled circuit subassembly, said first NMOS transistor being conducting and said second NMOS transistor being off as an ESD current entering into said first power supply, said first NMOS transistor being off and said second NMOS transistor being conducting as an ESD current entering into said second power supply.

12. (original) The device as recited in claim 11, wherein said RC controlled circuit subassembly further comprising:

a second capacitor, one end of said second capacitor being coupled to the high voltage source of said second power supply; and

a second resistance, coupled to the low voltage source of said first power supply and the other end of said second capacitor, together with said second capacitor, utilizing for substantially controlling said second NMOS transistor to be ON or OFF.

13. (original) The device as recited in claim 12, wherein the RC time constant of said second resistance and said second capacitor is about 0.1 to 10  $\mu\text{sec}$ .

14. (original) The device as recited in claim 12, wherein the gate of said second NMOS transistor is coupled between said second capacitor and said second resistance, the drain of said second NMOS transistor being coupled to the high voltage source of said second power supply, the source of said second NMOS transistor being coupled to the high voltage source of said first power supply.

15. (original) The device as recited in claim 11, wherein said first NMOS transistor is further located in a first P-well.

16. (original) The device as recited in claim 11, wherein said second NMOS transistor is further located in a second P-well.

17. (previously presented) An electrostatic discharge (ESD) protection device, applied to a mixed voltage circuit assembly, said device comprising:

- a RC controlled circuit subassembly, coupled with said mixed voltage circuit assembly, comprising a resistance and a capacitor, the RC time constant of said resistance and said capacitor is between a rise time of an electrostatic discharge and a rise time of said mixed voltage circuit assembly on a normal power-on condition, utilizing for substantially controlling said ESD protection device to be ON or OFF;

- a first PMOS transistor, coupled between a first power supply and a second power supply of said mixed voltage circuit assembly, wherein the gate of said first PMOS transistor is coupled between said resistance and said capacitor, and the source of said first PMOS transistor is coupled to the high voltage source of said first power supply; and

- a second PMOS transistor located in a second N-well, the gate of said second PMOS transistor being coupled to the low voltage source of said second power supply, the source of said second PMOS transistor and said second N-well being coupled to the drain of said first PMOS transistor, the drain of said second PMOS transistor being coupled to the high voltage source of said second power supply. .

18. (original) The device as recited in claim 17, wherein one end of said resistance is coupled to the high voltage source of said first power supply, and said capacitor is coupled to the

low voltage source of said second power supply and the other end of said resistance, and the RC time constant of said resistance and said capacitor is about 0.1 to 10  $\mu$ sec, utilizing for substantially controlling said first PMOS transistor to be ON or OFF.

19. (original) The device as recited in claim 17, wherein said first PMOS transistor is further located in a first N-well, said first N-well being coupled to the high voltage source of said first power supply.

20. (previously presented) The device as recited in claim 19, wherein said second PMOS transistor located in a second N-well and said second N-well being coupled to the drain of said first PMOS transistor.

21. (previously presented) An electrostatic discharge (ESD) protection device, applied to a mixed voltage circuit assembly, said device comprising:

- a RC controlled circuit subassembly, coupled with said mixed voltage circuit assembly, comprising a first resistance and a first capacitor, the RC time constant of said first resistance and said first capacitor is between a rise time of an electrostatic discharge and a rise time of said mixed voltage circuit assembly on a normal power-on condition, utilizing for substantially controlling said ESD protection device to be ON or OFF;

- a first NMOS transistor, coupled between a first power supply and a second power supply of said mixed voltage circuit assembly, wherein the gate of said first NMOS transistor is coupled between said resistance and said capacitor, and the drain of said first NMOS transistor is coupled to the high voltage source of said first power supply, and the source of said first NMOS transistor is coupled to the high voltage source of said second power supply;

- a second capacitor, one end of said second capacitor being coupled to the high voltage source of said second power supply;

- a second resistance, being coupled to the low voltage source of said first power supply and the other end of said second capacitor; and

- a second NMOS transistor, coupled between said first power supply and said second power supply of said mixed voltage circuit assembly, wherein said second NMOS transistor is coupled between said second capacitor and said second resistance, said first NMOS transistor

being conducting and said second NMOS transistor being off as an ESD current entering into said first power supply, said first NMOS transistor being off and said second NMOS transistor being conducting as an ESD current entering into said second power supply.

22. (original) The device as recited in claim 21, wherein one end of said first capacitor is coupled to the high voltage source of said first power supply, and said first resistance is coupled to the low voltage source of said second power supply and the other end of said capacitor, and the RC time constant of said first resistance and said first capacitor is about 0.1 to 10  $\mu$ sec, utilizing for substantially controlling said first NMOS transistor to be ON or OFF.

23. (original) The device as recited in claim 21, wherein said first NMOS transistor is further located in a P-well, said P-well, located in a N-well, being coupled to the high voltage source of said second power supply.

24. (canceled)

25. (previously presented) The device as recited in claim 21, wherein the RC time constant of said second resistance and said second capacitor is about 0.1 to 10  $\mu$ sec.

26. (previously presented) The device as recited in claim 21, wherein the gate of said second NMOS transistor is coupled between said second capacitor and said second resistance, the drain of said second NMOS transistor being coupled to the high voltage source of said second power supply, the source of said second NMOS transistor being coupled to the high voltage source of said first power supply.

27. (previously presented) The device as recited in claim 21, wherein said first NMOS transistor is further located in a first P-well.

28. (previously presented) The device as recited in claim 21, wherein said second NMOS transistor is further located in a second P-well.